

FIG. 5b

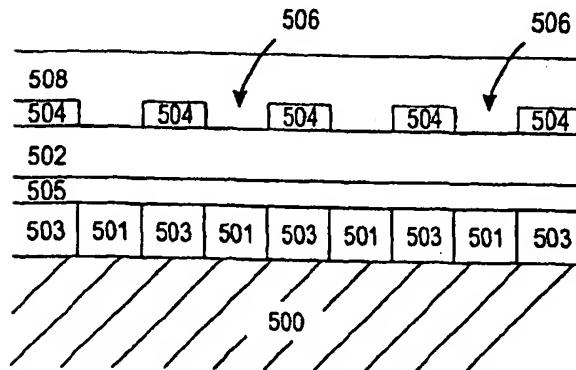


FIG. 5c

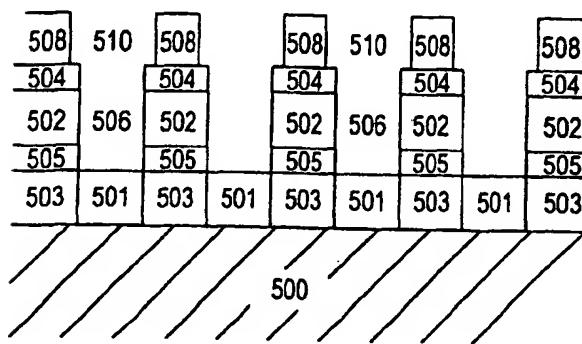


FIG. 5d

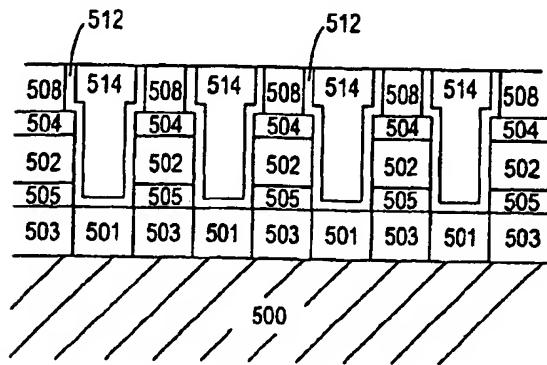


FIG. 5e

Description

[0001] The present invention relates to organosilicate layers, their use in integrated circuit fabrication, and a method for forming an organosilicate layer.

5 [0002] Integrated circuits have evolved into complex devices that can include millions of components (e. g., transistors, capacitors and resistors) on a single chip. The evolution of chip designs continually requires faster circuitry and greater circuit density. The demands for greater circuit density necessitate a reduction in the dimensions of the integrated circuit components.

10 [0003] As the dimensions of the integrated circuit components are reduced (e. g., sub-micron dimensions), the materials used to fabricate such components contribute to their electrical performance. For example, low resistivity metal interconnects (e. g., copper and aluminum) provide conductive paths between the components on integrated circuits. Typically, the metal interconnects are electrically isolated from each other by an insulating material. When the distance between adjacent metal interconnects and/or the thickness of the insulating material has sub-micron dimensions, capacitive coupling potentially occurs between such interconnects. Capacitive coupling between adjacent metal interconnects may cause cross talk and/or resistance-capacitance (RC) delay which degrades the overall performance of the integrated circuit. In order to prevent capacitive coupling between adjacent metal interconnects, low dielectric constant (low k) insulating materials (e. g., dielectric constants less than about 4.5) are needed.

15 [0004] The demands for greater integrated circuit densities also impose demands on the process sequences used for integrated circuit manufacture. For example, in process sequences using conventional lithographic techniques, a layer of energy sensitive resist is formed over a stack of material layers on a substrate. Many of these underlying material layers are reflective to ultraviolet light. Such reflections can distort the dimensions of features such as lines and vias that are formed in the energy sensitive resist material.

20 [0005] One technique proposed to minimize reflections from an underlying material layer uses an anti-reflective coating (ARC). The ARC is formed over the reflective material layer prior to resist patterning. The ARC suppresses the reflections off the underlying material layer during resist imaging, providing accurate pattern replication in the layer of energy sensitive resist.

25 [0006] Thereafter, the patterns formed in the energy-sensitive resist material are typically transferred into the underlying material layers. A hardmask layer is often used between the energy-sensitive resist layer and the underlying material layers to facilitate pattern transfer into the underlying material layers.

30 [0007] Therefore, a need exists in the art for low dielectric constant materials suitable for integrated circuit fabrication. Particularly desirable would be a low dielectric constant material that is also suitable as an ARC, and/or a hardmask.

[0008] A method of forming an organosilicate layer for use in integrated circuit fabrication is provided. In one embodiment, the organosilicate layer is formed by reacting a gas mixture comprising a phenyl-based alkoxy silane compound. The gas mixture comprising the phenyl-based alkoxy silane compound may be reacted by applying an electric field thereto. The gas mixture may optionally include an organosilane compound, an oxidizing gas, and/or an inert gas.

35 [0009] The organosilicate layer is compatible with integrated circuit fabrication processes. In one integrated circuit fabrication sequence, the organosilicate layer is used as an anti-reflective coating (ARC) for DUV lithography. For such an embodiment, a preferred process sequence includes forming the organosilicate layer on a substrate. The organosilicate layer has a refractive index (n) in a range of about 1.20 to about 1.70 and an absorption coefficient (κ) in a range of about 0.1 to about 0.7 at wavelengths less than about 250 nm. The refractive index (n) and the absorption coefficient (κ) of the organosilicate layer are tunable, in that they can be varied in the desired range as a function of the deposition temperature as well as the gas composition used during layer formation. After the organosilicate layer is formed on the substrate, a layer of energy sensitive resist material is formed thereon. A pattern is defined in the energy sensitive resist at a wavelength less than about 250 nm. Thereafter, the pattern defined in the energy sensitive resist material is transferred into the organosilicate layer. After the organosilicate layer is patterned, such pattern is optionally transferred into the substrate using the organosilicate ARC layer as a hardmask.

40 [0010] In another integrated circuit fabrication process, the organosilicate layer is incorporated into a damascene structure. For such an embodiment, a preferred process sequence includes depositing a first dielectric layer on a substrate. An organosilicate layer is then formed on the first dielectric layer. Thereafter, the organosilicate layer is patterned and etched to define contacts/vias therethrough. After the organosilicate layer is patterned and etched, a second dielectric layer is deposited thereover. The second dielectric layer is then patterned and etched to define interconnects therethrough. The interconnects formed in the second dielectric layer are positioned over the contacts/vias formed in the organosilicate layer. After the interconnects are formed the contacts/vias defined in the organosilicate layer are etched through the first dielectric layer to the substrate surface using the organosilicate layer as a hardmask.

45 [0011] Thereafter, the damascene structure is completed by filling the interconnects and contacts/vias with a conductive material.

50 [0012] The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a schematic illustration of an apparatus that can be used for the practice of embodiments described herein;

FIG. 2 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) chamber;

FIGS. 3a-3e depict schematic cross-sectional views of a substrate at different stages of integrated circuit fabrication incorporating an organosilicate layer as an anti-reflective coating (ARC);

FIGS. 4a-4e depict schematic cross-sectional views of a substrate at different stages of integrated circuit fabrication incorporating an organosilicate layer as a hardmask; and

FIGS. 5a-5e depict schematic cross-sectional views of a damascene structure at different stages of integrated circuit fabrication incorporating an organosilicate layer in such structure.

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[0012] FIG. 1 is a schematic representation of a wafer processing system 35 that can be used to perform integrated circuit fabrication in accordance with embodiments described herein. This apparatus typically comprises process chambers 36, 38, 40, 41, load-lock chambers 46, a transfer chamber 50, a microprocessor controller 54, along with other hardware components such as power supplies (not shown) and vacuum pumps (not shown). An example of such a wafer processing system 35 is a CENTURA® System, commercially available from Applied Materials, Inc., Santa Clara, California.

[0013] Details of the wafer processing system 35 used in the present invention are described in U.S. Pat. No. 5,186,718. The salient features of this system 35 are briefly described below.

[0014] The wafer processing system 35 includes a transfer chamber 50, containing a transfer robot 51. The transfer chamber 50 is coupled to load-lock chambers 46 as well as a cluster of process chambers 36, 38, 40, 41.

[0015] Substrates (not shown) are loaded into the wafer processing system 35 through load-lock chambers 46. Thereafter, transfer robot 51 moves the substrates between one or more of the process chambers 36, 38, 40, 41.

[0016] The process chambers 36, 38, 40, 41 are used to perform various integrated circuit fabrication sequences. For example, process chambers 36, 38, 40, 41 may include physical vapor deposition (PVD) chambers, ionized metal plasma physical vapor deposition (IMPPVD) chambers, chemical vapor deposition (CVD) chambers, rapid thermal process (RTP) chambers, and anti-reflective coating (ARC) chambers, among others.

[0017] FIG. 2 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) process chamber 36 of wafer processing system 35. CVD process chamber 36 may be used to deposit organosilicate layers in accordance with embodiments described herein. An example of such a CVD process chamber 36 is a DXZ™ chamber, commercially available from Applied Materials, Inc., Santa Clara, California.

[0018] CVD process chamber 36 typically comprises a gas panel 130, a control unit 110, along with other hardware components such as power supplies and vacuum pumps. Details of the CVD process chamber 36 are described in U.S. patent application Serial No. 09/211,998. The salient features of the CVD process chamber 36 are briefly described below.

[0019] The CVD process chamber 36 generally houses a support pedestal 150, which is used to support a substrate such as a semiconductor wafer 190. This pedestal 150 can typically be moved in a vertical direction inside the chamber 36 using a displacement mechanism (not shown). Depending on the specific process, the wafer 190 can be heated to some desired temperature prior to layer deposition. For example, the wafer support pedestal 150 is heated by an embedded heater element 170. The pedestal 150 may be resistively heated by applying an electric current from an AC power supply 106 to the heater element 170. The wafer 190 is, in turn, heated by the pedestal 150.

[0020] A temperature sensor 172, such as a thermocouple, is also embedded in the wafer support pedestal 150 to monitor the temperature of the pedestal 150 in a conventional manner. The measured temperature is used in a feedback loop to control the power supply 106 for the heating element 170, such that the wafer temperature can be maintained or controlled at a desired temperature which is suitable for the particular process application. The pedestal 150 is optionally heated using a plasma or by radiant heat (not shown).

[0021] A vacuum pump 102, is used to evacuate the process chamber 36 and to maintain the proper gas flows and pressure inside the chamber 36. A showerhead 120, through which process gases are introduced into the chamber 36, is located above the wafer support pedestal 150. The showerhead 120 is connected to a gas panel 130, which controls and supplies various gases used in different steps of the process sequence.

[0022] The showerhead 120 and wafer support pedestal 150 also form a pair of spaced apart electrodes. When an electric field is generated between these electrodes, the process gases introduced into the chamber 36 are ignited into a plasma. Typically, the electric field is generated by coupling the wafer support pedestal 150 to a source of RF power (not shown) through a matching network (not shown). Alternatively, the RF power source and matching network may be coupled to the showerhead 120, or coupled to both the showerhead 120 and the wafer support pedestal 150.

[0023] Plasma enhanced chemical vapor deposition (PECVD) techniques promote excitation and/or disassociation of the reactant gases by the application of the electric field to the reaction zone near the substrate surface, creating a plasma of reactive species. The reactivity of the species in the plasma reduces the energy required for a chemical reaction to take place, in effect lowering the required temperature for such PECVD processes.

[0024] In at least one embodiment, organosilicate layer deposition is accomplished by plasma enhanced oxidation of a phenyl-based silane compound containing one or more alkoxy-functional groups, such as phenyltrietoxysilane. The phenyl-based alkoxy silane compound is introduced into the process chamber 36 under the control of gas panel 130 as a gas with a regulated flow.

5 [0025] Proper control and regulation of the gas flows through the gas panel 130 is performed by mass flow controllers (not shown) and a computer (not shown). The showerhead 120 allows process gases from the gas panel 130 to be uniformly introduced and distributed in the process chamber 100.

10 [0026] Referring to FIG. 1, the CVD process chamber 36 is controlled by a microprocessor controller 54. The microprocessor controller 54 may be one of any form of general purpose computer processor (CPU) that can be used in an industrial setting for controlling various chambers and sub-processors. The computer may use any suitable memory, such as random access memory, read only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU for supporting the processor in a conventional manner. Software routines as required may be stored in the memory or executed by a second CPU that is remotely located.

15 [0027] The software routines are executed after the substrate is positioned on the pedestal. The software routine, when executed, transforms the general purpose computer into a specific process computer that controls the chamber operation so that a chamber process is performed. Alternatively, the process of the present invention may be performed in hardware, as an application specific integrated circuit or other type of hardware implementation, or a combination of software or hardware.

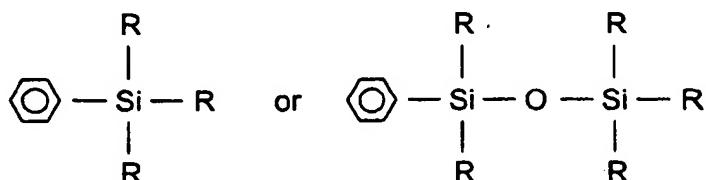
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Organosilicate Layer Deposition

25 [0028] In one embodiment, the organosilicate layer is formed by reacting a gas mixture comprising a phenyl-based alkoxy silane compound. The phenyl-based alkoxy silane compound has the general formula

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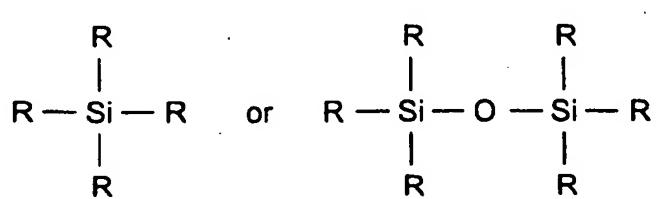
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wherein R may comprise an $O_xC_yH_z$ substituent, such that x has a range between 0 and 3, y has a range between 0 and 6, and z has a range between 1 and 30. For example, phenyltrietoxysilane ($SiO_3C_{12}H_{20}$), phenyltrimethoxysilane ($SiO_3C_9H_{14}$), diphenyldietoxysilane ($SiO_2C_{16}H_{20}$), and diphenyldimethoxysilane ($SiO_2C_{14}H_{16}$), among others may be used as the phenyl-based alkoxy silane compound.

40 [0029] The gas mixture may optionally include an organosilane compound having the general formula

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55 [0029] The gas mixture may optionally include an organosilane compound having the general formula

wherein R may comprise an $O_xC_yH_z$ substituent, such that x has a range between 0 and 3, y has a range between 0 and 6, and z has a range between 1 and 30. Trimethylsilane (SiC_3H_{10}), methylsilane ($SiCH_6$), triethylsilane (SiC_6H_{16}), dimethylsilane (SiC_2H_6), tetramethylsilane (SiC_4H_{12}), methoxysilane ($SiCH_6O$), dimethyldimethoxysilane ($SiC_4H_{12}O_2$), diethyldietoxysilane ($SiC_6H_{20}O_2$), dimethyldietoxysilane ($SiC_6H_{16}O_2$), diethyldietoxysilane ($SiC_6H_{16}O_2$), hexamethyldisiloxane ($Si_2C_6H_{18}O$), bis(methylsilano)methane ($Si_2C_3H_{12}$), 1,2-bis(methylsilano)ethane ($Si_2C_4H_{14}$), among

others, may be used as the organosilane compound.

[0030] Additionally, the gas mixture may optionally include an oxygen-containing gas. Oxygen (O₂), ozone (O₃), nitrous oxide (N₂O), carbon monoxide (CO), carbon dioxide (CO₂), or combinations thereof, among others, may be used as the oxygen-containing gas.

5 [0031] The gas mixture may also include an inert gas. Argon (Ar), helium (He), neon (Ne), xenon (Xe), nitrogen (N₂), and combinations thereof, among others may be used as the inert gas.

[0032] In general, the following deposition process parameters can be used to form the organosilicate layer using a CVD process chamber similar to that shown in FIG. 2. The process parameters may include a wafer temperature of about 50 °C to about 500 °C, a chamber pressure of about 1 torr to about 500 torr, a phenyl-based alkoxy silane compound gas flow rate of about 10 milligrams/minute (mgm) to about 1500 mgm, an organosilane compound flow rate of about 10 sccm to about 2000 sccm, an oxygen-containing gas flow rate of about 10 sccm to about 2000 sccm, an inert gas flow rate of about 1 sccm to about 10000 sccm, and an RF power of between about 1 watts/cm² to about 1500 watts/cm². The above process parameters provide a deposition rate for the organosilicate layer in the range of about 500 Å/min to about 20000 Å/min when implemented on a 200 mm (millimeter) substrate in a deposition chamber available from Applied Materials, Inc., Santa Clara, California.

10 [0033] Other deposition chambers are within the scope of the invention, and the parameters listed above may vary according to the particular deposition chamber used to form the organosilicate layer. For example, other deposition chambers may have a larger (e.g. configured to accommodate 300 mm substrates) or smaller volume, requiring gas flow rates that are larger or smaller than those recited for deposition chambers available from Applied Materials, Inc.

15 [0034] The as-deposited organosilicate layer has a dielectric constant that is less than about 3.0, making it suitable for use as an insulating material in integrated circuits. The dielectric constant of the organosilicate layer is tunable, in that it can be varied in the desired range as a function of the reaction temperature. In particular, as the temperature increases the dielectric constant of the as-deposited layer decreases.

20 [0035] The dielectric constant of the organosilicate layer can also be tuned as a function of the composition of the gas mixture during layer formation. As the carbon (C) concentration in the gas mixture increases, the C content of the as-deposited organosilicate layer similarly increases, decreasing its dielectric constant.

25 [0036] The organosilicate layer also has an absorption coefficient that is tunable in a range of about 0.1 to about 0.7 at wavelengths less than about 250 nm. The absorption coefficient is tunable as a function of the reaction temperature. In particular, as the temperature increases the absorption coefficient of the as-deposited layer increases.

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Integrated Circuit Fabrication Processes

A. Organosilicate Anti-Reflective Coating (ARC)

35 [0037] FIGs. 3a-3e illustrate schematic cross-sectional views of a substrate 300 at different stages of an integrated circuit fabrication sequence incorporating an organosilicate layer as an anti-reflective coating (ARC). In general, the substrate 300 refers to any workpiece on which film processing is performed, and a substrate structure 350 is used to generally denote the substrate 300 together with other material layers formed on the substrate 300. Depending on the specific stage of processing, the substrate 300 may correspond to a silicon wafer, or other material layer, which has been formed on the substrate. FIG. 3a, for example, illustrates a cross-sectional view of a substrate structure 350 in which the substrate 300 is a silicon wafer.

40 [0038] An organosilicate layer 302 is formed on the substrate structure 350. The organosilicate layer 302 is formed on the substrate structure 350 according to the process parameters described above. The organosilicate layer has an absorption coefficient (κ) that can be varied between about 0.1 to about 0.7 at wavelengths below about 250 nm (nanometers), making it suitable for use as an anti-reflective coating (ARC) at deep ultraviolet (DUV) wavelengths. The absorption coefficient of the organosilicate layer is tunable, in that it can be varied in the desired range as a function of the deposition temperature as well as the carbon concentration in the gas mixture during layer formation. The thickness of the organosilicate layer 302 is variable depending on the specific stage of processing. Typically, the organosilicate layer has a thickness of about 200 Å to about 2000 Å.

45 [0039] FIG. 3b depicts a layer of energy sensitive resist material 304 formed on the substrate structure 350 of FIG. 3a. The layer of energy sensitive resist material may be spin coated on the substrate structure 350 to a thickness within a range of about 2000 Å to about 6000 Å. The energy sensitive resist material is sensitive to DUV radiation having a wavelength less than about 250 nm.

50 [0040] An image of a pattern is introduced into the layer of energy sensitive resist material 304 by exposing such energy sensitive resist material 304 to DUV radiation via mask 306. When the image of the pattern is introduced into the layer of energy sensitive resist material 304, the organosilicate layer 302 suppresses any reflections off underlying material layers (e. g., oxides, metals). Such reflections can degrade the image of the pattern introduced in the layer of energy sensitive resist material 304.

[0041] The image of the pattern introduced into the layer of energy sensitive resist material 304 is developed in an appropriate developer to define the pattern therethrough, as shown in FIG. 3c. Thereafter, referring to FIG. 3d, the pattern defined in the energy sensitive resist material 304 is transferred through the organosilicate layer 302. The pattern is transferred through the organosilicate layer 302 using the energy sensitive resist material 304 as a mask.

5 The pattern is transferred through the organosilicate layer 302 by etching it using an appropriate chemical etchant (e.g., carbon tetrafluoride (CF₄) or a gas mixture comprising trifluoromethane, fluoroethane, or fluorobutene (CHF₃) and oxygen (O₂)).

[0042] Fig. 3e illustrates the completion of the integrated circuit fabrication sequence by the transfer of the pattern defined in the organosilicate layer 302 into the substrate 300. The pattern is transferred into the substrate 300 using 10 the organosilicate layer 302 as a hardmask. The pattern is transferred into the substrate 300 by etching the substrate 300 using an appropriate chemical etchant (e.g., CF₄).

[0043] After the substrate 300 is patterned, the organosilicate layer 302 can optionally be stripped from the substrate structure 350 by etching it using an appropriate chemical etchant (e.g., carbon tetrafluoride CF₄), or a gas mixture comprising trifluoromethane (CHF₃) and oxygen (O₂).

15 B. Organosilicate Hardmask

[0044] FIGS. 4a-4e illustrate schematic cross-sectional views of a substrate 400 at different stages of an integrated circuit fabrication sequence incorporating an organosilicate layer as a hard mask. In general, the substrate 400 refers 20 to any workpiece on which processing is performed, and the substrate structure 450 is used to generally denote the substrate together with other material layers formed on the substrate 400. Depending on the specific stage of processing, the substrate 400 may correspond to a silicon substrate, or other material layer that has been formed on the substrate. FIG. 4a, for example, illustrates a cross-sectional view of a substrate structure 450, having a material layer 402 formed thereon. The material layer 402 may be an oxide (e.g., silicon dioxide). In general, the substrate 400 may 25 include a layer of silicon, silicides, metals, or other materials. FIG. 4a illustrates one embodiment in which the substrate 400 is silicon having a silicon dioxide layer formed thereon.

[0045] FIG. 4b depicts an organosilicate layer 404 formed on the substrate structure 450 of FIG. 4a. The organosilicate layer 404 is formed on the substrate structure 450 according to the process parameters described above. The thickness of the organosilicate layer 400 is variable depending on the specific stage of processing. Typically, the organosilicate layer 404 is deposited to a thickness of about 200 Å to about 2000 Å.

[0046] A layer of energy sensitive resist material 408 is formed on the organosilicate layer 404. The layer of energy sensitive resist material 408 can be spin coated on the substrate to a thickness within a range of about 4,000 Å to about 10,000 Å. Most energy sensitive resist materials are sensitive to ultraviolet (UV) radiation having a wavelength less than about 450 nm (nanometers). Deep ultraviolet (DUV) resist materials are sensitive to UV radiation having 35 wavelengths less than about 245 nm.

[0047] Dependent upon the etch chemistry of the energy sensitive resist material 408 used in the fabrication sequence, an intermediate layer 406 is formed on the organosilicate layer 404 prior to the layer of energy sensitive resist material 408. When the energy sensitive resist material 408 and the organosilicate layer 404 can be etched using the same chemical etchants, the intermediate layer 406 functions as a mask for the organosilicate layer 404. The intermediate layer 406 may be conventionally formed on the organosilicate layer 404. The intermediate layer 406 may be an oxide, nitride, silicon oxynitride, amorphous silicon, or other suitable material.

[0048] An image of a pattern is introduced into the layer of energy sensitive resist material 408 by exposing such energy sensitive resist material 408 to DUV radiation via mask 410. The image of the pattern introduced in the layer of energy sensitive resist material 408 is developed in an appropriate developer to define the pattern therethrough, as 45 shown in FIG. 4c.

[0049] Thereafter, referring to FIG. 4d, the pattern defined in the energy sensitive resist material 408 is transferred through the organosilicate layer 404 using the energy sensitive resist material 408 as a mask. The pattern is transferred through the organosilicate layer 404 using an appropriate chemical etchant. For example, fluorocarbon compounds such as carbon tetrafluoride (CF₄), fluoroethane (C₂F₆), and fluorobutene (C₄F₈) may be used to chemically etch the 50 organosilicate layer 404.

[0050] Alternatively, when the intermediate layer 406 is present, the pattern defined in the energy sensitive resist material 408 is first transferred through the intermediate layer 406 using the energy sensitive resist material 408 as a mask. Thereafter, the pattern is transferred through the organosilicate layer 404 using the intermediate layer 406 as a mask. The pattern is transferred through both the intermediate layer 406 as well as the organosilicate layer 404 using 55 the appropriate chemical etchants.

[0051] FIG. 4e illustrates the completion of the integrated circuit fabrication sequence by the transfer of the pattern defined in the organosilicate layer 404 through the silicon dioxide layer 402 using the organosilicate layer 404 as a hardmask.

[0052] After the silicon dioxide layer 402 is patterned, the organosilicate layer 404 can optionally be stripped from the substrate 400 by etching it using a suitable chemical etchant.

5 C. Damascene Structure Incorporating an Organosilicate Layer

[0053] FIGS. 5a-5e illustrate schematic cross-sectional views of a substrate 500 at different stages of a damascene structure fabrication sequence incorporating an organosilicate layer therein. Damascene structures are typically used to form metal interconnects on integrated circuits. Depending on the specific stage of processing, substrate 500 may correspond to a silicon substrate, or other material layers that have been formed on the substrate 500. FIG. 5a, for example, illustrates a cross-sectional view of a substrate 500 having conductive features 501, intermetal dielectric 503, a barrier layer 505, as well as a first dielectric layer 502 formed thereon. The conductive features 501 may be a metal (e. g., aluminum, copper). The intermetal dielectric 503 and the barrier layer 505 may be a low dielectric constant material (e. g., organosilicate material, silicon carbide). The first dielectric layer 502 may be an oxide (e. g., silicon dioxide, fluorosilicate glass). In general, the substrate 500 may include a layer of silicon, silicides, metals, or other materials.

[0054] FIG. 5a illustrates one embodiment in which the substrate 500 is silicon, the conductive features 501 are copper, the intermetal dielectric 503 silicon oxide, and the first dielectric layer 502 is a fluorosilicate glass. The first dielectric layer 502 has a thickness of about 1,000 Å to about 10,000 Å, depending on the size of the structure to be fabricated.

20 [0055] An organosilicate layer 504 is formed on the first dielectric layer 502. The organosilicate layer 504 is formed on the first dielectric layer 502 according to the process parameters described above. The organosilicate layer 504 has a dielectric constant less than about 3.0, so as to prevent or minimize capacitive coupling between the metal interconnects to be formed in the damascene structure. The dielectric constant for the organosilicate layer is tunable, in that it can be varied in the desired range as a function of the reaction temperature as well as the composition of the gas mixture during layer formation.

25 [0056] The thickness of the organosilicate layer 504 is variable depending on the specific stage of processing. Typically, the organosilicate layer 504 has a thickness of about 200 Å to about 1000 Å, depending on its dielectric-constant as well as its etch selectivity with respect to an overlying dielectric material subsequently formed thereon (e. g., the barrier layer preferably has an etch selectivity with respect to the overlying dielectric layer that is greater than about 10:1).

30 [0057] Referring to FIG. 5b, the organosilicate layer 504 is patterned and etched to define contact/via openings 506 and to expose the first dielectric layer 502, in areas where the contacts/vias are to be formed. The contact/via openings 506 are positioned over the conductive features 501. The organosilicate layer 504 is patterned using conventional lithography (as described above with reference to FIGS. 4b-4d) and etched using fluorocarbon compounds such as fluoromethane (CF₄), fluoroethane (C₂F₆), fluorobutene (C₄F₈), and combinations thereof.

35 [0058] After the organosilicate layer 504 is patterned, a second dielectric layer 508 is deposited over the organosilicate layer 504, as shown in FIG. 5c. The second dielectric layer 508 may be an oxide (e. g., silicon dioxide, fluorosilicate glass). The second dielectric layer 508 has a thickness of about 1,000 Å to about 10,000 Å, depending on the size of the structure to be fabricated.

40 [0059] The second dielectric layer 508 is then patterned to define interconnects 510, as illustrated in FIG. 5d, preferably using conventional lithography processes as described above. The interconnects 510 formed in the second dielectric layer 508 are positioned over the contact/via openings 506 in the organosilicate layer 504. Thereafter, both the interconnects 510 and contacts/vias 506 are etched to expose the surface of the conductive features 501, using reactive ion etching or other anisotropic etching techniques.

45 [0060] Referring to FIG. 5e, the interconnects 510 and contacts/vias 506 are filled with a conductive material 514 such as aluminum (Al), copper (Cu), tungsten (W), or combinations thereof. Typically, copper is used to fill the interconnects 510 and contacts/vias 506 due to its low resistivity (resistivity about 1.7 $\mu\Omega\text{-cm}$). The conductive material 514 is deposited using chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof, to form the damascene structure. Preferably, a barrier layer 512 such as tantalum, tantalum nitride, or other suitable barrier material is first deposited conformably on the sidewalls of the interconnects 510 and contacts/vias 506 to prevent metal migration into the surrounding dielectric layers 502, 508 as well as the organosilicate layer 504.

55 Claims

1. A method of thin film deposition, comprising:

positioning a substrate in a deposition chamber;

providing a gas mixture to the deposition chamber, wherein the gas mixture comprises a phenyl-based alkoxysilane compound; and
 reacting the gas mixture to form an organosilicate layer on the substrate.

5 2. The method of claim 1 wherein the thin film deposition comprises forming an organosilicate layer on a substrate.

3. A method of forming a device, comprising:

10 forming an organosilicate layer on a substrate,
 wherein the organosilicate layer is formed by reacting a gas mixture comprising a phenyl-based alkoxysilane compound in a deposition chamber; and
 defining a pattern in at least one region of the organosilicate layer.

15 4. The method of claim 3 further comprising transferring the pattern defined in the at least one region of the organosilicate layer into the substrate using the organosilicate layer as a mask.

5. The method of claim 3 or 4 further comprising the step of removing the organosilicate layer from the substrate.

20 6. The method of claim 1 to 3 wherein the substrate has one or more material layers formed thereon.

25 7. The method of claim 3 wherein definition of the pattern in at least one region of the organosilicate layer, comprises:

25 forming a layer of energy sensitive resist material on the organosilicate layer;
 introducing an image of the pattern into the layer of energy sensitive resist material by exposing the energy sensitive resist material to patterned radiation;
 developing the image of the pattern introduced into the layer of energy sensitive resist material; and
 transferring the pattern through the organosilicate layer using the layer of energy sensitive resist material as a mask.

30 8. The method of claim 7 further comprising:

35 forming an intermediate layer on the organosilicate layer prior to forming the layer of energy sensitive resist thereon, introducing the image of a pattern therein, and developing the pattern;
 transferring the image of the pattern developed in the layer of energy sensitive resist material through the intermediate layer using the energy sensitive resist material as a mask; and
 transferring the pattern through the organosilicate layer using the intermediate layer as a mask.

39 9. The method of claim 8 wherein the intermediate layer is an oxide the oxide being preferably selected from the group of silicon dioxide, fluorosilicate glass (FSG), and silicon oxynitride.

40 10. The method of claim 5 wherein the organosilicate layer is removed from the substrate using a fluorine-based compound the fluorine-based compound being preferably selected from the group of carbon tetrafluoride (CF₄), fluoromethane (CFH₃), fluoroethane (C₂F₆), fluorobutene (C₄F₈), and combinations thereof.

45 11. The method of claim 3 wherein the organosilicate layer is an anti-reflective coating at wavelengths less than about 250 nm (nanometers).

12. A method of fabricating a damascene structure, comprising:

50 forming a first dielectric layer on a substrate;
 forming an organosilicate layer on the first dielectric layer, wherein the organosilicate layer is formed by reacting a gas mixture comprising a phenyl-based alkoxysilane compound in a deposition chamber;
 patterning the organosilicate layer to define contacts/vias therethrough;
 forming a second dielectric layer on the patterned organosilicate layer;
 55 patterning the second dielectric layer to define interconnects therethrough, wherein the interconnects are positioned over the contacts/vias defined in the organosilicate layer;
 etching the first dielectric layer to form contacts/vias therethrough; and
 filling the contacts/vias and the interconnects with a conductive material.

13. The method of claim 12 wherein the first dielectric layer and the second dielectric layer are each selected from the group consisting of amorphous carbon, fluorinated amorphous carbon, parylene, fluorinated silicate glass (FSG), AF_4 , BCB, silicon carbide, oxynitride, and combinations thereof.

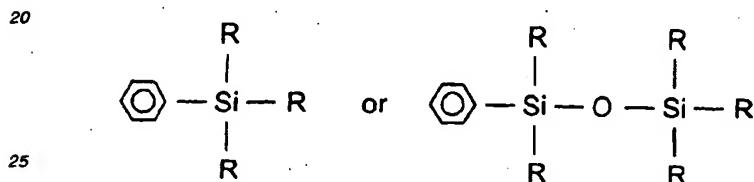
5 14. The method of claim 12 wherein the conductive material filling the contacts/vias and interconnects is selected from the group of copper (Cu), aluminum (Al), tungsten (W), and combinations thereof.

15. The method of claim 12 wherein the gas mixture further comprises an oxygen-containing gas.

10 16. The method of claim any of the claim 1 to 3 or 12 wherein the gas mixture is reacted by applying an electric field to the gas mixture in the deposition chamber.

17. The method of claim any of the claim 1 to 3 or 12 wherein the gas mixture further comprises an organosilane compound.

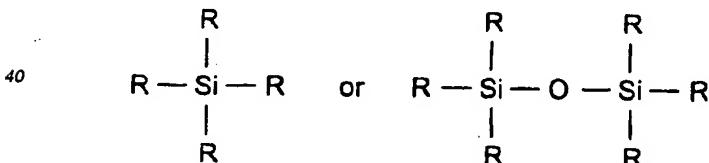
15 18. The method of claim any of the claim 1 to 3 or 12 wherein the phenyl-based alkoxy silane compound has the general formula



wherein R comprises an $O_xC_yH_z$ constituent, and wherein x has a range between 0 and 3, y has a range between 0 and 6, and z has a range between 1 and 30.

30 19. The method of claim 18 wherein the phenyl-based alkoxy silane compound is selected from the group of phenyl-triethoxysilane ($SiO_3C_{12}H_{20}$), phenyltrimethoxysilane ($SiO_3C_9H_{14}$), diphenyldiethoxysilane ($SiO_2C_{16}H_{20}$), diphenyldimethoxysilane ($SiO_2C_{14}H_{16}$), and combinations thereof.

35 20. The method of claim 17 wherein the organosilane compound has the general formula



45 wherein R comprises an $O_xC_yH_z$ substituent, and wherein x has a range between 0 and 3, y has a range between 0 and 6, and z has a range between 1 and 30.

21. The method of claim 20 wherein the organosilane compound is selected from the group of trimethylsilane (SiC_3H_{10}), triethylsilane (SiC_6H_{16}), methylsilane ($SiCH_6$), dimethylsilane (SiC_2H_8), tetramethylsilane (SiC_4H_{12}), methoxysilane ($SiCH_6O$), dimethyldimethoxysilane ($SiC_4H_{12}O_2$), diethylidethoxysilane ($SiC_8H_{20}O_2$), dimethylidethoxysilane ($SiC_6H_{16}O_2$), diethylidethoxysilane ($SiC_6H_{16}O_2$), hexamethyldisiloxane ($Si_2C_6H_{18}O$), bis(methylsilano)methane ($Si_2C_3H_{12}$), 1,2-bis(methylsilano)ethane ($Si_2C_4H_{14}$), and combinations thereof.

50 22. The method of claim any of the claim 1 to 3 or 12 wherein the gas mixture further comprises an oxygen-containing gas, the oxygen-containing gas being preferably selected from the group of nitrous oxide (N_2O), oxygen (O_2), ozone (O_3), carbon monoxide (CO), carbon dioxide (CO_2), and combinations thereof.

55 23. The method of claim 16 wherein the electric field applied to the gas mixture in the deposition chamber is a radio

frequency (RF) power, the RF power being preferably within the range of about 1 watts/cm² to about 1500 watts/cm².

- 5 24. The method of claim any of the claim 1 to 3 or 12 wherein the deposition chamber is maintained at a pressure between about 1 torr to about 500 torr.
- 10 25. The method of claim any of the claim 1 to 3 or 12 wherein the phenyl-based alkoxysilane compound is provided to the deposition chamber at a flow rate in a range of about 10 mgm (milligrams/minute) to about 1500 mgm.
- 15 26. The method of any of the claim 1 to 3 or 12 wherein the organosilane compound is provided to the deposition chamber at a flow rate in a range of about 10 sccm to about 2000 sccm.
- 20 27. The method of claim 22 wherein the oxygen-containing gas is provided to the deposition chamber at a flow rate in a range of about 10 sccm to about 2000 sccm.
- 25 28. The method of claim any of the claim 1 to 3 or 12 wherein the deposition chamber is maintained at a temperature between about 50 °C to about 500 °C.
- 30 29. The method of claim any of the claim 1 to 3 or 12 wherein the gas mixture further comprises an inert gas, the inert gas being preferably selected from the group of helium (He), argon (Ar), neon (Ne), xenon (Xe), nitrogen (N₂), and combinations thereof.
- 35 30. The method of claim 29 wherein the inert gas is provided to the deposition chamber at a flow rate in a range of about 1 sccm to about 10000 sccm.
- 40 31. The method of any of the preceding claims wherein the organosilicate layer has an absorption coefficient in a range of about 0.1 to about 0.7 at wavelengths less than about 250 nm.
- 45 32. The method of any of the preceding claims wherein the organosilicate layer has a dielectric constant less than about 3.0.
- 50 33. The method of any of the preceding claims wherein the organosilicate layer has an index of refraction in a range of about 1.2 to about 1.7.
- 55 34. A computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber according to a method as claimed in any of preceding claims.

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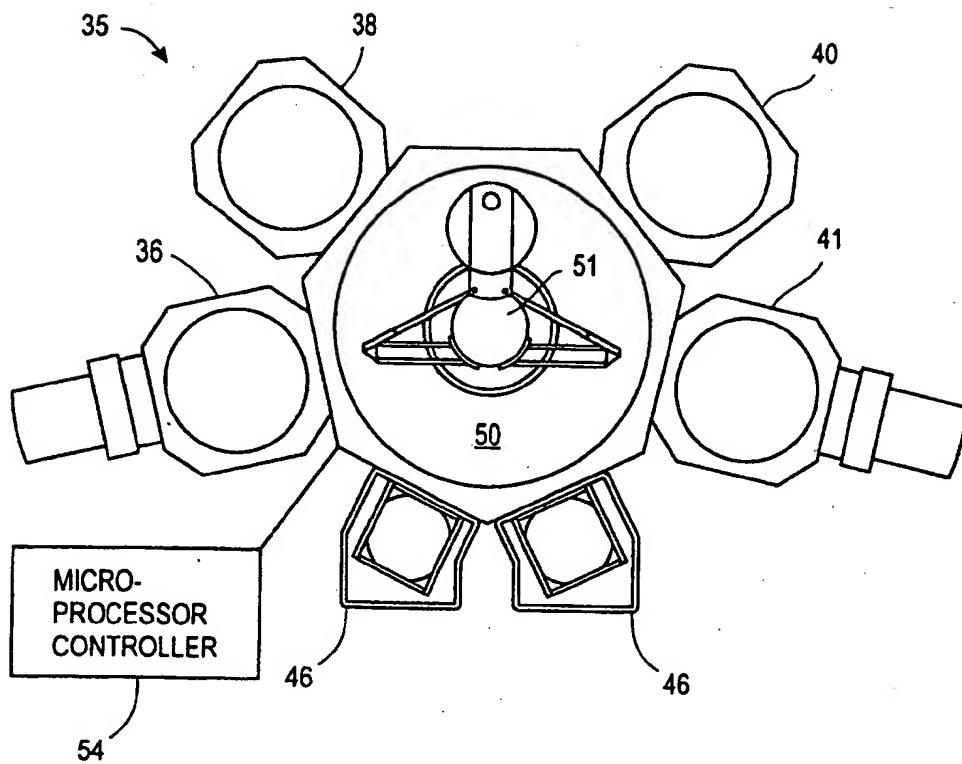


FIG. 1

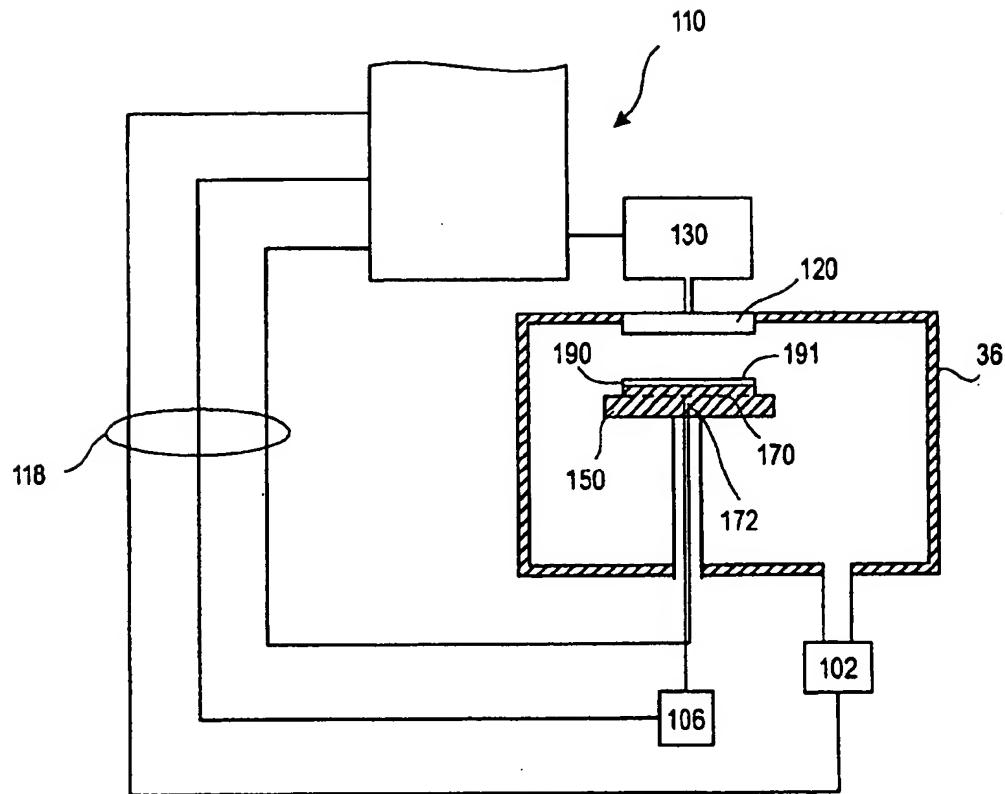


FIG. 2

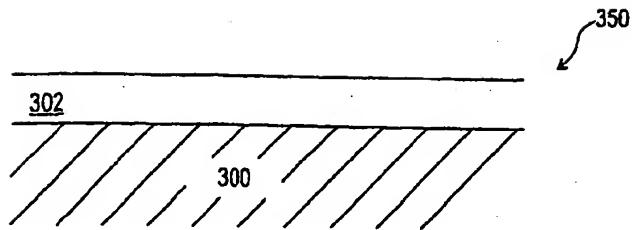


FIG. 3a

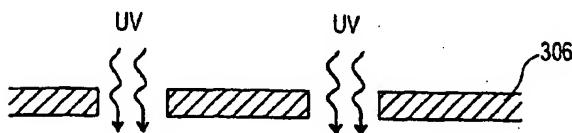


FIG. 3b

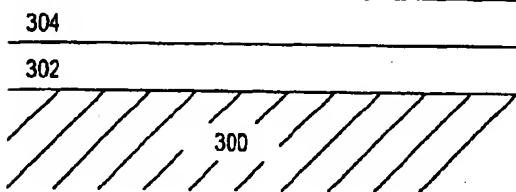


FIG. 3c

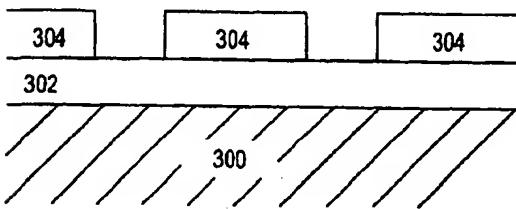


FIG. 3d

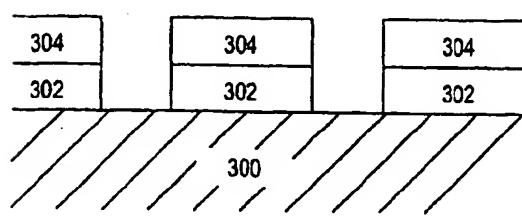


FIG. 3e

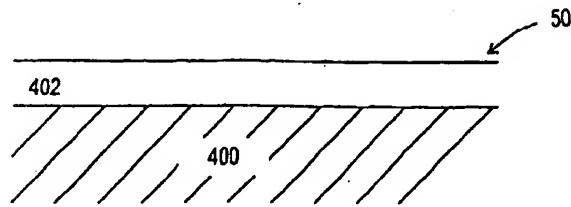


FIG. 4a

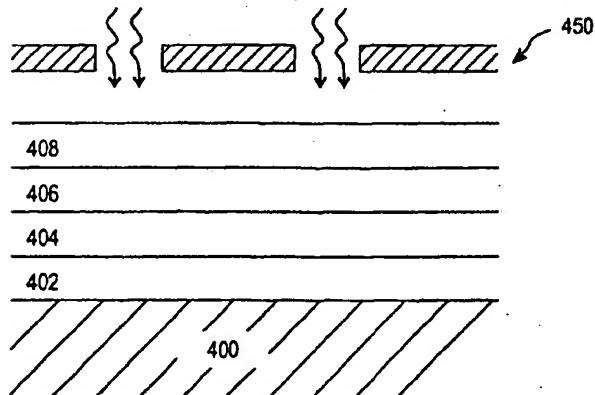


FIG. 4b

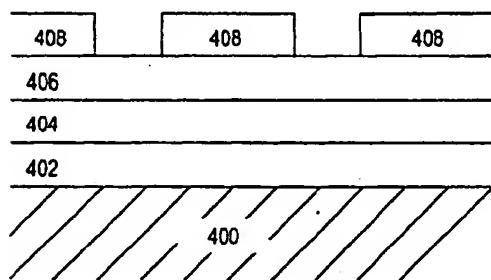


FIG. 4c

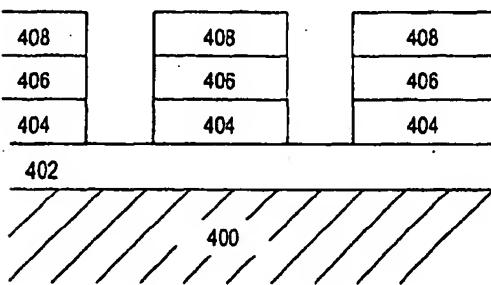


FIG. 4d

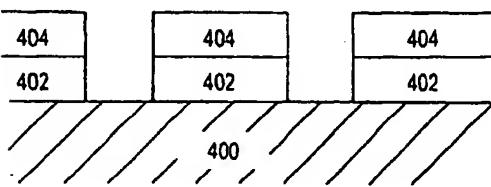


FIG. 4e

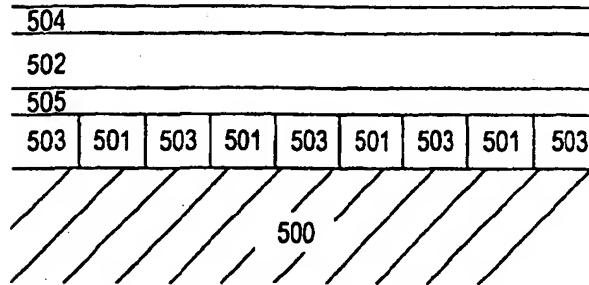


FIG. 5a

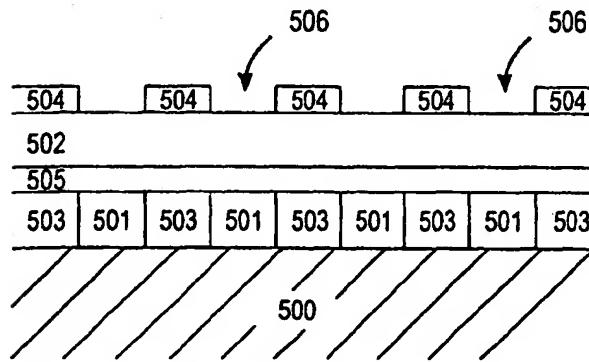


FIG. 5b

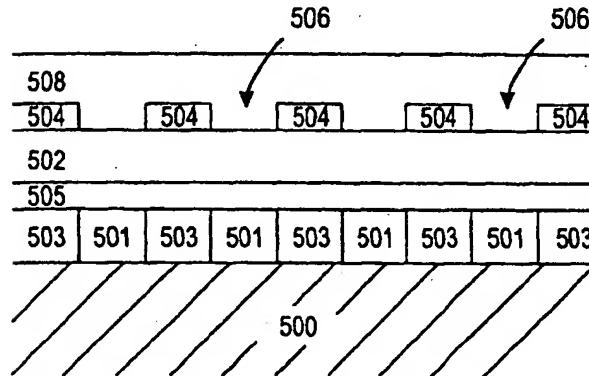


FIG. 5c

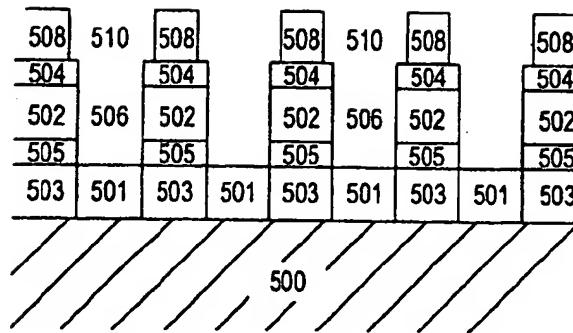


FIG. 5d

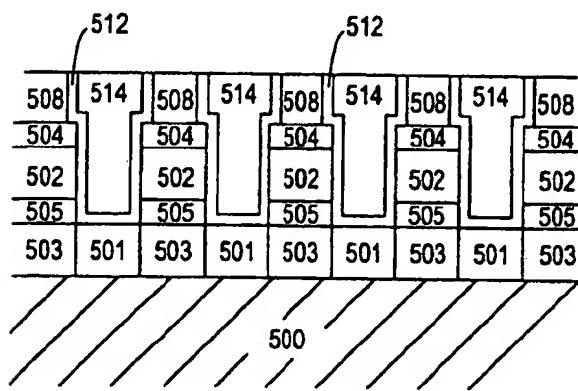


FIG. 5e

